On Accumulator-Based Bit-Serial Test Response Compaction Schemes

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Abstract

The data paths of most contemporary general and special purpose processors include registers, adders and other arithmetic circuits. If these circuits are also used for Built-In Self-Test, the extra area required for embedding testing structures can be cut down efficiently. Several schemes based on accumulators, subtracters, multipliers and shift registers have been proposed and analyzed in the past for parallel test response compaction, whereas some efforts have also been devoted in the bit-serial response compaction case. In this paper, we analyze and evaluate the bit-serial version of a recently proposed scheme for parallel test response compaction [5]. Experimental results on the ISCAS'85 benchmark circuits indicate that the post-compaction fault coverage drop attained by the new scheme is significantly lower than other already known accumulator-based compaction schemes.

1. Introduction

The advances of semiconductor process technology force IC companies to move towards very deep submicron integrated circuit technology for taking advantage of the increased functionality, higher speeds and decreased costs that it offers. Very deep submicron ICs although capable of offering increased speed and integration of millions of gates require new and effective test methodologies in order to be tested adequately and cost effectively.

Built-In Self-Test (BIST) is becoming a very attractive Design For Testability (DFT) strategy since it reduces external testing requirements. BIST tries to incorporate in the same IC the Circuit Under Test (CUT) and its tester enabling in this way the chip to test itself. Although this leads to increased implementation area, this DFT method is becoming more and more attractive since it decreases the time to market, it often leads to higher testing quality and it cuts down the cost effectively [1].

The quality of a BIST scheme depends on: (a) the Test Pattern Generator (TPG), a circuit that produces the patterns applied to the CUT, and (b) the Test Response Verifier, a circuit that captures the responses of the CUT, compacts them to one single pattern called the *signature* and compares this against the signature of a fault-free CUT.

Even if the test pattern sequence generated by the TPG achieves 100% fault coverage for a specific fault model, the post compaction fault coverage may be much smaller due to the well-known problem of *aliasing*. Aliasing is the possibility that a faulty and a fault-free circuit produce the same signature although the CUT's output responses differ.

The silicon area required for embedding BIST can be minimized if some of the original building blocks of the circuit are utilized to generate patterns and / or to compact test responses. Processor as well as digital signal processing circuits' datapaths contain adders, subtractors and multipliers. The suitability of these circuits for test response compaction in test per-clock BIST schemes has been investigated in [2-5]. In several cases however, the use of a test per-scan scheme, that is bit-serial pattern generation and compaction, is imperative. For example, we can refer to: (a) embedded cores with an isolation ring, (b) circuits with a boundary scan path and (c) sequential circuits with scan paths.

The suitability of various arithmetic circuits for bit-serial test pattern generation and test response compaction was investigated in [6]. Serial bit compaction by an accumulator using either a 2's complement adder or a rotate carry adder was discussed. Finally, the author of [6] proposed the use of a serial-parallel response compaction scheme and derived an upper bound on the limiting value of the aliasing probability for efficiently long test sequences. In many cases however, the length of the test set may not be very large. In such cases, the actual aliasing ratio may be far larger than the upper bound derived in [6] and the post-compaction fault coverage may drop below

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the acceptable levels. Experiments performed on the ISCAS'85 benchmark circuits verified our fears (experimental results will be presented in Section 3). Recently, a new test response compaction scheme based on an accumulator behaving as a multiple-input Non-Linear Feedback Shift Register has been proposed [5]. It has been shown that this scheme achieves significantly lower post-compaction fault coverage drop than the other accumulator-based test response compaction schemes in test-per-clock BIST. However its effectiveness in test-per-scan structures has not been investigated. In this work we investigate its suitability for serial test response compaction. Experiments on the ISCAS'85 circuits reveal its superiority against the already known accumulator-based bit-serial schemes.

In the next section we review the bit-serial and serial-parallel response compaction schemes that have already been proposed and we analyze the bit-serial versions of the parallel scheme proposed in [5]. We also compare these schemes in terms of area overhead. Experimental results on the ISCAS'85 circuits are presented in Section 3. Conclusions are given in the last section.

2. Bit Serial Response Compaction Schemes

Consider a CUT which has x outputs and y, with $y \geq 0$ (in case of a combinational circuit $y = 0$), internal state flip-flops connected in a single scan path. The response of the CUT is shifted out serially by the application of x + y cycles of a shift clock, suppose S_c. Finally, suppose that the width of the available accumulator is k.

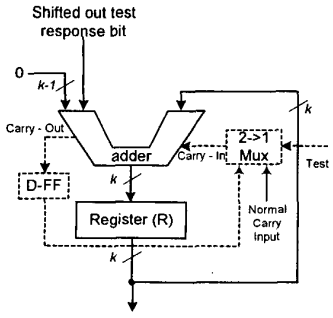

Figure 1. Bit-serial Accumulator response compactors.

A first bit-serial response compactor [6] based on the bit-parallel compactor presented in [3] is shown in Figure 1 (ignore the dashed lines logic). We will denote this scheme as "bit-serial accumulator". Each response bit that is shifted out is added at the least significant bit position, in order for all the bits of the signature to get affected by possible erroneous responses. For small test lengths and large accumulator widths (k = 32 or 64) this is equivalent to a counter of 1s of the test responses whereas for smaller values of k and large test lengths the response compactor of Figure 1 is equivalent to a modulo 2^k counter of 1s. Provided that an accumulator exists in the original system, this scheme does not impose any area overhead.

A second bit-serial response compactor [6] can be derived based on the bit-parallel compactor presented in [2]. The modifications required by this scheme against the previous one are indicated by the dashed lines in Figure 1. The carry-out of the adder is stored in a flip-flop and added to the contents of the register in the next S_c cycle. The area overhead in this case is very small and composed of a D flip-flop and a multiplexer controlled by the Test mode signal for selecting the input (normal carry input or the output of the D flip-flop) at the Carry-In. We will denote this compactor as "bit-serial accumulator with stored carry feedback".

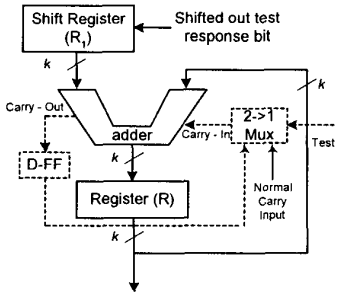

Figure 2. Serial-Parallel response compactors.

In the above schemes, if due to a fault the amount of +1 bit errors equals the number of −1 errors, the fault will not be detected since the bits of the responses are added using the same weight. This can be alleviated if the i-th response bit is added at position i mod k of the accumulator as suggested by [6]. A straightforward implementation of this scheme is given in Figure 2. In this scheme, after k bits of the response have been shifted in the shift register R_1, the content of R_1 is added with the content of R. The sum is stored in R. We will denote these response compactor as "serial-parallel accumulator", implying that the response of the CUT is first shifted in a k-bits wide register. Again, two different compactors one with stored carry feedback and one without carry feedback may be constructed in an analogous to Figure 1 way. According to the analysis of [6] it is expected that these response compactors would perform better than those of Figure 1.

However, the area overhead that the scheme of Figure 2 imposes depends on the existence of a second register. If such a register exists, the area overhead imposed consists of the required gates for converting it into a shift register. If a second register is not available in the original system, a k-bit shift register needs to be added. Moreover, since an addition takes place after k new response bits have been shifted into R_1, a new clock signal must be devised with a period of $k*S_c$ clocks. For deriving such a signal the introduction of a $\lceil \log_2 k \rceil$ bits wide counter will be required.

Recently, test response compaction by an accumulator behaving as a multiple-input Non-Linear Feedback Shift Register has been proposed in [5]. The parallel scheme proposed in [5] can easily be modified to a bit-serial test response compaction scheme by restricting the number of output response bits that are processed at each clock cycle to one (see Figure 3). In test mode, during each clock cycle, the contents of the register are shifted by one position to the left and are added with the operand A of the adder and the content of the D flip-flop (denoted as X). The result of the addition is stored back in the register and the X flip-flop. The final content of the register constitutes the signature. Note that the least significant bit of A is the output response bit of the CUT while the remaining k-1 bits are at constant values during testing.

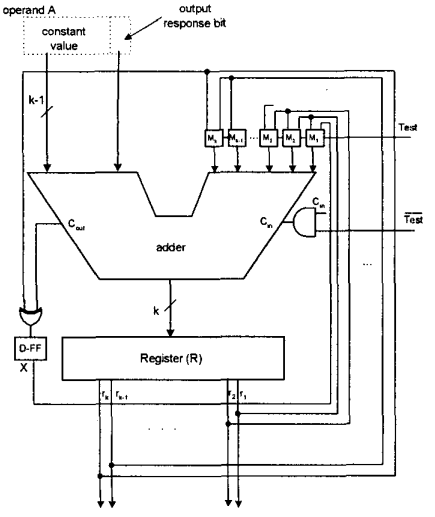

Figure 3. Proposed bit-serial response compactor.

The accumulator of Figure 3 in test mode functions as the Non-Linear Feedback Shift Register of Figure 4. We can see that a constant value (denoted as $a_{k-1}...a_2a_1$) is applied at the k-1 most significant bits. Taking into account the carry generation functions of an adder, we get: $c_i = c_{i-1}a_{i-1} + c_{i-1}r_{i-1} + a_{i-1}r_{i-1}$, for i=2,...,k where r_i is used to denote the contents of the corresponding shift register cell. If $a_{i-1} = 0$ then $c_i = c_{i-1}r_{i-1}$ whereas if $a_{i-1} = 1$ then $c_i = c_{i-1} + r_{i-1}$. Therefore, depending on the value of bit a_i, the feedback logic that drives cell D_i is equivalent to an AND or an OR logic gate. Giving the same logic value to all k-1 bits of the constant value, all feedbacks in Figure 4 implement the same function. (AND or OR logic function). In LFSR-based test response compaction schemes the accepted truth in order to reduce error masking is to make the divisor polynomial reasonably complex [p.139 of 8]. Similarly, in our scheme we expect that, by applying a constant value with an irregular pattern of zeros and ones, we will achieve a post-compaction fault coverage drop smaller than by applying a regular pattern.

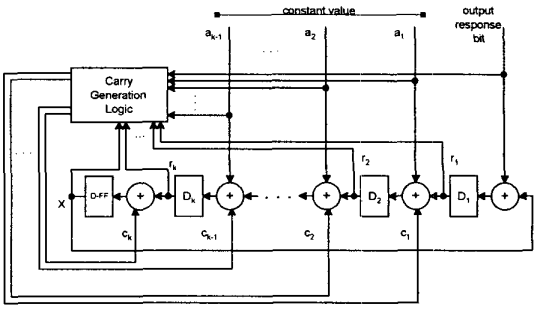

Figure 4. The accumulator behaving as a Single Input Non-Linear Feedback Shift Register.

The area overhead imposed by the proposed scheme is dominated by the multiplexer insertion and is equivalent with that needed for converting an existing register of the circuit into a shift register. Note that in the proposed compactor no extra clock signal is required since a new addition is performed in every S_c clock cycle in a bit serial fashion. Therefore, the area overhead for the modifications required by the proposed scheme is less than that of Figure 2, but increased compared to the response compactors of Figure 1. However, as we will show with experimental results, the compactors of Figure 1 are incapable of sustaining the post-compaction fault coverage at high levels.

3. Evaluation and Comparisons

In order to validate the effectiveness of the proposed scheme, we performed several simulations. We use a customized fault simulator that implements the various response compaction schemes and computes the signatures for all single stuck-at faults in the CUT.

For our experiments we use the non-redundant version of the ISCAS'85 benchmark circuits. These circuits are combinational parts of datapaths and are therefore likely to be accompanied by an accumulator. We consider that the registers of the inputs and outputs of the circuits form a scan path.

We also consider two test sets :

- Deterministic compacted test sets derived using the Test Synthesis tools by Synopsys. We assume that the test vectors of these test sets are serially applied to the scan register of the circuit.
- Pseudorandom test sets produced by LFSRs. For each benchmark circuit we choose a primitive polynomial of degree m (m = 25 or 31 in our experiments) based on the guidelines given in [9] and construct the corresponding LFSR. We feed the scan register of the circuit with the output of the LFSR until we achieve the desired fault coverage (100% or less in the cases of circuits with random pattern resistant faults).

Table 1. Number of vectors and pre-compaction Fault Covarage for the ISCAS'85 circuits

	Deterministic Test Set		*Pseudorandom Test Set*	
	Vectors	*Pre-Compaction FC*	*Vectors*	*Pre-Compaction FC*
c432nr	52	100%	379	100%
c499nr	59	100%	640	100%
c880nr	49	100%	5385	100%
c1355nr	86	100%	1358	100%
c1908nr	117	100%	5138	100%
c2670nr	92	100%	396	83.53%
c3540nr	206	100%	2044	99.71%
c5315nr	114	100%	1423	100%
c6288nr	27	100%	59	100%
c7552nr	162	100%	766	95.05%

The number of vectors in each test set used as well as the pre-compaction fault coverage for each circuit are given in Table 1.

At first we evaluate the bit-serial response compaction schemes proposed in [6], that is the bit-serial accumulator with and without stored carry feedback and the serial-parallel accumulator with and without stored carry feedback. Table 2 presents results for three different datapath sizes (k=8, 16 or 32).

From the results of Table 2 we can see that:

- The post-compaction fault coverage drop in the bit-serial accumulator scheme is very high in the case of compacted test sets for the ISCAS'85 benchmark circuits. It is smaller in the case of pseudorandom test sets but still remains at high levels.
- For small accumulators (k=8), there are some cases where the bit-serial accumulator without carry feedback gives slightly better results than the bit-serial accumulator with stored carry feedback.
- The bit-serial accumulator with stored carry feedback gives the same results with the bit-serial accumulator without stored carry feedback for large accumulators (k=16 and 32). This can be justified by the fact that these response compaction schemes implement a one's count function and therefore a carry is unlikely to happen in cases of a few hundred or thousand test vectors. When the size of the accumulator is small (e.g. k=8) or the test set consists of several thousand test vectors, then the two schemes may lead to different results.

Table 2. Post-Compaction Fault Coverage Drop for the bit-serial response compaction schemes presented in [6]

	bit-serial accumulator without carry feedback			**bit-serial accumulator with stored carry feedback**			**serial-parallel accumulator without carry feedback**			**serial-parallel accumulator with stored carry feedback**		
	k=8	***k=16***	***k=32***	***k=8***	***k=16***	***k=32***	***k=8***	***k=16***	***k=32***	***k=8***	***k=16***	***k=32***
	Deterministic Test Sets											
c432nr	7.40%			7.40%			2.63%	1.91%		1.91%		
c499nr	2.75%			2.75%			3.87%	1.83%	1.02%	0.61%	0.31%	
c880nr	4.72%			4.72%			10.97%	6.70%	2.39%	2.39%		
c1355nr	18.11%			18.11%			12.21%	9.73%	8.91%	9.28%	8.17%	8.18%
c1908nr	7.52%			7.52%			8.07%	4.69%	4.09%	4.98%	4.19%	4.09%
c2670nr	22.75%			22.75%			8.53%	5.16%	4.84%	5.03%	4.81%	4.72%
c3540nr	7.77%			7.77%			2.60%	0.60%	0.48%	0.92%	0.53%	0.48%
c5315nr	8.01%			8.01%			3.63%	2.00%	0.95%	1.04%	0.67%	0.65%
c6288nr	8.25%			8.25%			2.31%	1.77%	1.36%	0.99%	0.96%	
c7552nr	4.97%	4.95%		4.95%			9.73%	4.80%	4.28%	4.03%	3.95%	3.85%
	Pseudorandom Test Sets											
c432nr	0.48%			0.48%			4.42%	0.12%		0.12%		
c499nr	6.92%			6.92%			6.72%	3.46%	2.95%	2.14%		
c880nr	0.74%			0.85%	0.74%		7.56%	3.35%	0.34%	0.51%	0.28%	
c1355nr	3.82%			3.82%			4.49%	2.90%	2.15%	2.08%	1.34%	
c1908nr	1.29%			1.34%	1.29%		6.88%	1.64%	0.95%	1.13%	0.95%	
c2670nr	2.98%			2.98%			4.03%	1.66%	1.44%	1.27%	0.88%	
c3540nr	0.88%	0.78%		0.82%	0.78%		2.10%	0.18%	0.00%	0.25%	0.00%	
c5315nr	2.12%	2.10%		2.17%	2.10%		3.55%	1.19%	0.37%	0.48%	0.25%	0.23%
c6288nr	6.53%			6.53%			1.28%	0.80%	0.35%	0.13%	0.12%	
c7552nr	4.13%			4.15%	4.13%		10.65%	4.57%	4.19%	3.54%	3.45%	

- Furthermore, each one of the two schemes produces the same results for k=16 and 32 indicating that an increase in the size of accumulator will not lead to any better results.
- The serial-parallel schemes produce much better results compared to the bit-serial schemes. In this case, the scheme with the stored carry feedback achieves better results compared with the scheme without stored carry feedback and the results improve with larger accumulator sizes. However in many cases the post-compaction fault coverage drop is more than 1%.

We conclude that the above mentioned schemes are inadequate to provide small post-compaction fault coverage drop. We now evaluate the proposed scheme. In order to evaluate the effect of the constant value that is selected for the k-1 bits that are added together with the CUT's output response bit, we present results in Table 3 for 3 different values: (a) 0000..., (b) 0101... and (c) a random value.

We can easily see that, in all cases, the proposed scheme achieves far better results than the other accumulator-based schemes. We can also see that the value 0000..., as it was expected, is not the best choice for the k-1 bits. The other two values produce zero fault coverage drop in almost all cases, when k=16 or 32, and very small fault coverage drop in small accumulator sizes (eg. k=8).

The mean value of the post-compaction fault coverage drops measured on the ISCAS'85 circuits for various examined accumulator sizes is presented in Figure 5.

4. Conclusions

BIST approaches are gaining increasing interest in today's complex integrated circuits. There are several cases of circuit or sub-circuit BIST in which bit serial testing structures are more appropriate than their bit parallel counterparts. Cores with an isolation ring or scan path equipped sub-circuits are such examples. If these testing structures can be derived by slight modifications of already existent hardware then BIST can be added with a minimum implementation area increase.

In this paper we have analyzed and evaluated the already known schemes for bit-serial test response compaction and the bit-serial version of the parallel test response compaction scheme proposed in [5].

Experimental results on the ISCAS'85 benchmark circuits using both deterministic and pseudorandom test sets show that the proposed bit serial compactor's post-compaction fault coverage drop is significantly lower than the already known bit-serial or serial-parallel response compacting schemes. Moreover, the area required for the accumulator modifications is very small.

Table 3. Post-Compaction Fault Coverage Drop for the proposed bit-serial response compaction scheme

<table>
<tr><th></th><th colspan="3">value = 0000...</th><th colspan="3">value = 0101...</th><th colspan="3">random value</th></tr>
<tr><th></th><th>k=8</th><th>k=16</th><th>k=32</th><th>k=8</th><th>k=16</th><th>k=32</th><th>k=8</th><th>k=16</th><th>k=32</th></tr>
<tr><td></td><td colspan="9">Deterministic Test Sets</td></tr>
<tr><td>c432nr</td><td>0.00%</td><td>0.24%</td><td>0.00%</td><td>0.24%</td><td colspan="2" rowspan="8">0.00%</td><td>0.24%</td><td colspan="2" rowspan="9">0.00%</td></tr>
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<tr><td>c880nr</td><td>0.68%</td><td>0.17%</td><td>0.51%</td><td>0.51%</td><td>0.40%</td></tr>
<tr><td>c1355nr</td><td>0.63%</td><td>0.41%</td><td>0.56%</td><td>0.52%</td><td>0.45%</td></tr>
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<tr><td>c6288nr</td><td>0.32%</td><td>0.07%</td><td>0.10%</td><td>0.51%</td><td>0.00%</td><td>0.02%</td><td>0.43%</td></tr>
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<tr><td>c880nr</td><td>0.11%</td><td>0.45%</td><td>0.17%</td></tr>
<tr><td>c1355nr</td><td>0.37%</td><td>0.22%</td><td>0.33%</td></tr>
<tr><td>c1908nr</td><td>0.29%</td><td>0.21%</td><td>0.69%</td></tr>
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<tr><td>c5315nr</td><td>0.38%</td><td>0.31%</td><td>0.56%</td></tr>
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<tr><td>c7552nr</td><td>0.35%</td><td colspan="2">0.00%</td><td>0.42%</td><td>0.39%</td></tr>
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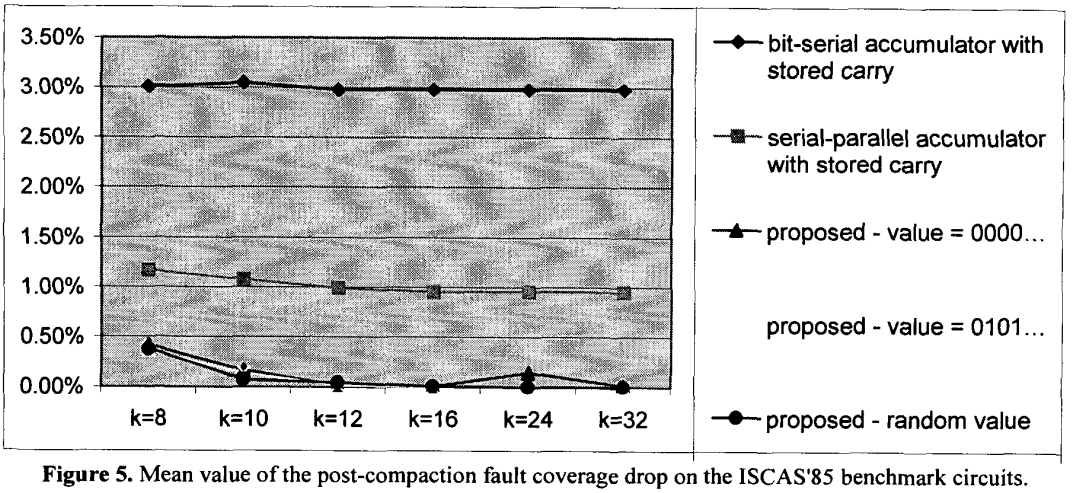

Figure 5. Mean value of the post-compaction fault coverage drop on the ISCAS'85 benchmark circuits.

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