On Path Delay Fault Testing of Multiplexer - Based Shifters

H. T. Vergos[1,2], Y. Tsiatouhas[3], Th. Haniotakis[3], D. Nikolos[1,2] & M. Nicolaidis[4]

[1]Dept. of Computer Engineering and Informatics, University of Patras, 26 500, Rio, Patras, Greece
e-mail : {vergos,nikolosd}@ cti.gr
[2]Computer Technology Institute, 3 Kolokotroni Str., 262 21 Patras, Greece
[3] ISD S.A, 22, K. Varnali Str, 152 33 Maroussi, Athens, Greece
e-mail :{haniotak, tsiatouhas}@isd.gr
[4]Reliable Integrated Systems Group, TIMA, 46, Avenue, Felix Viallet, 38031, Grenoble, France
michael.nicolaidis@imag.fr

Abstract

*In this paper we present a method for path delay fault testing of multiplexer-based shifters. We show that many paths of the shifter are non-robustly testable and we give a path selection method so as all the selected paths to be robustly testable by 20 * log_2n + 2 test-vector pairs, where n is the length of the shifter. The propagation delay along all other paths is a function of the delays along the selected paths.*

1. Introduction

Increasing performance requirements of the contemporary VLSI circuits makes it difficult to design them with large timing margins. Thus imprecise delay modeling, the statistical variations of the parameters during the manufacturing process as well as physical defects in the integrated circuits can degrade circuit performance without altering its logic functionality. The change in the timing behavior of the circuit is modeled by two popular fault models. One is the gate delay fault model where delays violating specifications are assumed to be due to a single gate delay [1, 2]. The other is the path delay fault model where a path is declared faulty if it fails to propagate a transition from the path input to the path output within a specified time interval [3]. The latter model is deemed to be more general since it captures the cumulative effect of small delay variations in gates along a path as well as the faults caused by a single gate. A physical path of a circuit is an alternating sequence of gates and lines leading from a primary input to a primary output of the circuit. The number of physical paths in a contemporary circuit is prohibitively large in order for all the paths to be tested for path delay faults. To this end to reduce the paths that must be tested for path delay faults various path selection methods have been proposed (for example [4 - 7]) although none of them has been proven to be satisfactory for the general case.

This work addresses the problem of shifters' path delay fault testing and is a part of a broader project concerning the path delay fault testing of all modules included in a data path (for example adders [7], multipliers, etc.) Data paths are essential and generally the biggest parts of microprocessors and microcontrollers. Shifters can be implemented in different formats; such as barrel-shifters or multiplexer based [8]. This work considers implementations using standard cells because they are becoming predominant in industrial context and also can be easily automated through the use of an HDL.

An n-bit multiplexer-based shifter capable of performing up to n-1 positions shift of its input operand in a single clock cycle is a combinational circuit made up of m = log_2n levels. Each level requires n building blocks and is capable of performing a shift function of 2^i positions according to the value of C_i, $i \in \{0, 1, \ldots, m-1\}$ which is the common control signal of each level. Each level accepts as inputs the outputs of the previous level (or the primary inputs) and only drives the subsequent level (or the primary outputs). A value of 0 at C_i indicates that no shifting will take place at the ith level of the shifter. Each function is selected according to the values of t_1t_0 signals as shown in Table 1. Every building block of the shifter accepts the same t_1t_0 signal values, thus it performs the same shift function every clock cycle.

We consider that the length n of the operand is a power of 2, that is, n = 8, 16, 32, 64, … Only in some very special cases, the length n may not be a power of 2. Figure

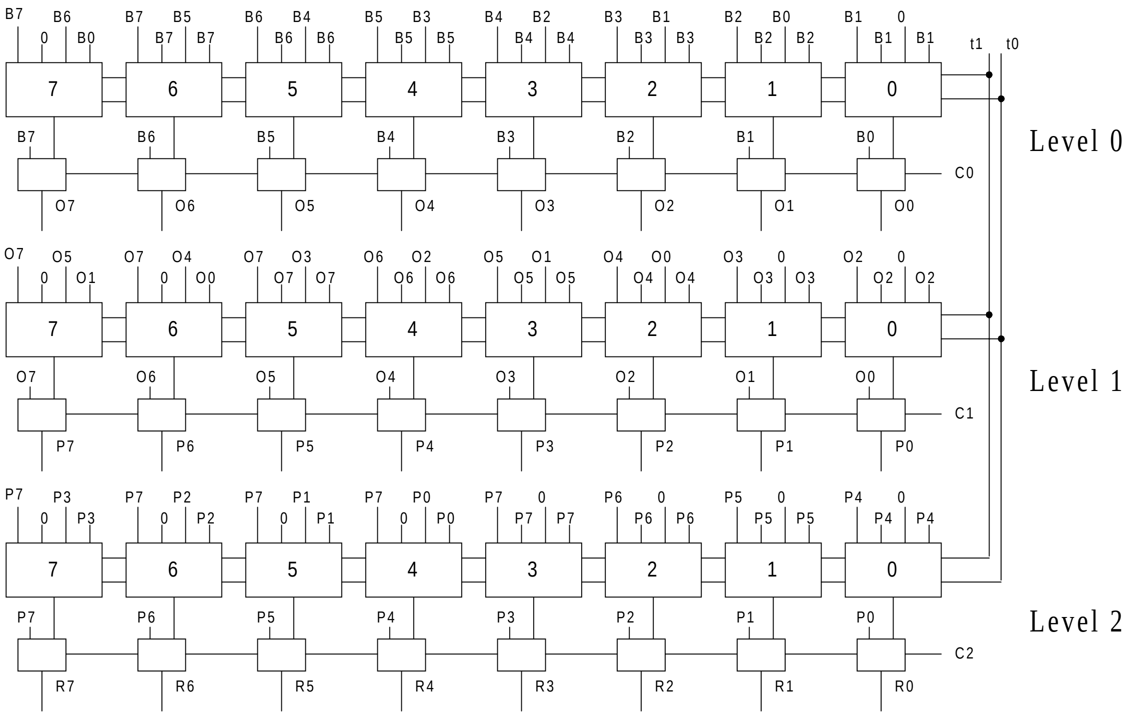

Figure 1. An 8-bit multiplexer - based shifter capable of performing 4 different shift functions.

Table 1. t_1t_0 signals functionality

t_1t_0	Operation
00	Rotate Right
01	Logical Left Shift
10	Logical Right Shift
11	Arithmetic Right Shift

1 presents a 8-bit multiplexer-based shifter capable of performing the four different functions indicated in Table 1. The routing between the various levels has been omitted for clarity. Lines that should be connected between the different levels have been named in a unique way. The basic building block of the shifter is composed of two multiplexers :

a. A 4 -> 1 multiplexer controlled by the t_1t_0 signals which implements the one out of four possible shift functions. When t_1t_0 have the 00 or 01 or 10 or 11 value the rightmost, the next to the rightmost, the next to the leftmost and the leftmost input of every 4->1 MUX are driven respectively to its output.
b. A 2->1 multiplexer controlled by the appropriate C_i signal.

2. Path Delay Fault Testing of the Shifter

During the normal operation of a multiplexer-based shifter, there are transitions at the data inputs, the control signals $C_{m-1}C_{m-2}\ldots C_1C_0$, as well as the function signals t_1t_0. This means that for path delay fault testing of the shifter, we must consider delay faults along paths that are driven from any of these possible sources.

We define a test session as the application of a pair of test vectors which sensitize a certain path and propagate a transition (0->1 or 1->0) of one of the inputs of the circuit to at least one of the outputs of the circuit for observation. We note that for each physical path two such test vectors always exist in a completely robustly testable circuit. If during a test session more than one distinct paths can be sensitized in parallel and made to propagate a transition to distinct primary outputs, then all these paths can be tested in parallel for path delay faults, thus reducing testing effort and the test application time significantly.

In a multiplexer-based shifter, we divide the possible physical paths in three different categories.

1st Category. Paths starting from the data inputs.

We define the paths established by a specific combination of the control signals $C_{m-1}C_{m-2}\ldots C_1C_0$ and the function signals t_1t_0 as a group of paths or simply group.

Lemma 1. The propagation delays along all the paths of a group can be measured in parallel.

Proof. a) The paths of each group defined by $t_1t_0 \in \{00, 01, 10\}$ and any value of the control signals $C_{m-1}C_{m-2}\ldots C_1C_0$ do not have any common sub-path. Thus propagation delays along these paths can be measured in parallel. b) The physical paths of each group, defined by t_1t_0=11 and any value of the control signals $C_{m-1}C_{m-2}\ldots C_1C_0$ may split into sub-paths that do not re-converge. Specifically each sub-path ends to a distinct primary output of the shifter. So the propagation delays along the paths of each one of these groups can be measured in parallel. ▪

As weight w of a group we define the number of ones in the combination of the control signals $C_{m-1}C_{m-2}\ldots C_1C_0$ that establishes the paths of this group. According to this definition it is evident that the groups with same $C_{m-1}C_{m-2}\ldots C_1C_0$ values and different t_1t_0 values have the same weight.

Theorem 1. For a specific value of t_1t_0 the propagation delay along any path P_1 in a group with weight $w_1>1$ can be calculated by the propagation delays along a path P_2 in a group with weight $w_2=w_1-1$, a path P_3 in a group with weight $w_3=1$ and a path P_4 in a group with weight $w_4=0$.

Proof. Let P_1 be a path with $w_1>1$ and $P_1=P_{1a}/P_{1b}$ where P_{1a} is a sub-path from the data operand input to the output of the first level i for which the corresponding control signal C_i is 1. Consider now the path $P_4=P_{4a}/P_{4b}$, where P_{4a} and P_{1a} end at the same point and P_4 belongs to the group with weight 0. Furthermore, consider the path $P_2=P_{2a}/P_{2b}$ where $P_{2a}=P_{4a}$ and $P_{2b}=P_{1b}$. Obviously, this path has a weight $w_2=w1-1$. Finally, consider the path P_3 with $P_3=P_{3a}/P_{3b}$ where $P_{3a}=P_{1a}$ and $P_{3b}=P_{4b}$. The weight of path P_3 is $w_3=1$. From the above analysis we can see that the propagation delay $d(P_1)$ along path P_1 can be expressed as a linear combination of the propagation delays $d(P_2)$, $d(P_3)$ and $d(P_4)$ along paths P_2, P_3 and P_4 respectively, as follows: $d(P_1) = d(P_2) + d(P_3) - d(P_4)$ ▪

Example 1. For the shifter of Figure 1 consider $t_1t_0 = 00$. Furthermore, consider the paths: $P_1=B_4\text{-}O_3/O_3\text{-}P_3/P_3\text{-}R_7$, established by C=101, that is, $w_1= 2$, with $P_{1a}=B_4\text{-}O_3$ and $P_{1b}=O_3\text{-}P_3/P_3\text{-}R_7$, $P_2=B_3\text{-}O_3/O_3\text{-}P_3/P_3\text{-}R_7$, established by C= 100, that is, $w_2=1$, with $P_{2a}=B_3\text{-}O_3$ and $P_{2b}=O_3\text{-}P_3/P_3\text{-}R_7$, $P_3=B_4\text{-}O_3/O_3\text{-}P_3/P_3\text{-}R_3$, established by C=001, that is, $w_3=1$, with $P_{3a}=B_4\text{-}O_3$ and $P_{3b}= O_3\text{-}P_3/P_3\text{-}R_3$, and $P_4=B_3\text{-}O_3/O_3\text{-}P_3/P_3\text{-}R_3$, established by C=000, that is, $w_4=0$, with $P_{4a}=B_3\text{-}O_3$ and $P_{4b}=O_3\text{-}P_3/P_3\text{-}R_3$. Then the propagation delay time along path P_1 can be expressed as : $d(P_1) = d(P_2)+d(P_3)- d(P_4)$.

Theorem 1 implies that the propagation delay along any path with weight w greater than 1 can be calculated from the propagation delays along a path with weight w-1, a path with weight 1 and a path with weight 0. The propagation delay along the path with weight w-1 can be calculated from the propagation delays along a path with weight w-2, a path with weight 1 and a path with weight 0. Thus by induction we conclude that if we measure the propagation delays along all paths in groups with weight 0 and 1, then we can calculate the propagation delays along any path with greater weight. The groups of paths with weight 0 are identical for any possible value of t_1t_0. Thus, the propagation delays along these paths should only be measured once.

The number of test sessions needed to measure the propagation delays along the paths of groups with weight 0 and 1 is equal to: $2 * (4 * \log_2 n + 1)$, where n is the length of the operand. For the shifter of Figure 1 the number of such test sessions is 26.

2nd Category. Paths starting from the control inputs $C_{m-1}C_{m-2}\ldots C_1C_0$.

Let L_i be the set of all paths starting from a control signal C_i with all other control signals $C_j=0$, $j\neq i$, and $t_1t_0=00$.

A path from a control signal C_i through a 2->1 MUX for which C_i is the control input, is established iff the inputs of the multiplexer have complementary values. Obviously there are two kinds of such paths from a control signal C_i through a 2->1 MUX for which C_i is the control input, the paths where the inputs of the multiplexer have the values 0 and 1 and the those where the inputs of the multiplexer have the values 1 and 0.

Consider now a control signal input C_i, and also that for every C_j, with $j\neq i$, $C_j=0$. Furthermore, consider that for the function signals we have the values $t_1t_0=00$. In order to achieve that the inputs of all 2->1 multiplexers at level i have complementary values, we divide the data operand inputs into two groups with complementary values between them. The first group is constructed from the data inputs numbered x, where $x \bmod 2^{i+1} < 2^i$, and the second group is constructed from the data inputs numbered y, where $y \bmod 2^{i+1} \geq 2^i$.

Example 2. Consider the control signal input C_2 in Figure 1. In order to achieve that the inputs of all 2->1 multiplexers at level 2, have complementary values we divide the data operand inputs into two groups, one group with the inputs $\{B_0, B_1, B_2, B_3\}$ and another group with the inputs $\{B_4, B_5, B_6, B_7\}$. These two groups should have complementary values. Furthermore, we must set $C_0C_1= 00$ and $t_1t_0=00$. To measure the propagation delay for each of the transitions of C_2, 0->1 and 1->0, we have to set $B_0=B_1=B_2=B_3=0$ and $B_4=B_5=B_6=B_7=1$ and then $B_0=B_1=B_2=B_3=1$ and $B_4=B_5=B_6=B_7=0$.

Lemma 2. The propagation delays along all paths starting from a control input C_i to the primary outputs of the shifter, with $C_j=0$ for every $j\neq i$ and $t_1t_0=00$, can be measured in parallel, for every one of the two combinations of complementary values for the two groups of data inputs.

Proof. Since $C_j=0$ for every $j\neq i$ all these paths do not have any common sub-path, thus the propagation delays along them can be measured in parallel. ▪

For every level i the number of test sessions in order to measure the propagation delays along the paths in set L_i is 4. Thus in order to measure the propagation delay times along the paths in all sets L_i, where $0 \leq i \leq m-1$, we need $4*m = 4*\log_2 n$ test sessions.

Theorem 2. If we measure the propagation delays along all the paths in set L_i, $0 \leq i \leq m-1$, then for every other path starting from C_i its propagation delay can be expressed as a linear combination of the propagation delays along paths in L_i and paths of the 1st category.

Proof. Let $P_1=P_{1a}/P_{1b}$ be a path starting from C_i, where P_{1a} is the sub-path from the input C_i to the output MO of the 2->1 multiplexer of level i. Furthermore consider the corresponding path $P_2=P_{2a}/P_{2b}$ in L_i with $P_{2a}=P_{1a}$. Next consider the path $P_3=P_{3a}/P_{3b}$ of the 1st category, where P_{3a} is the sub-path from the corresponding data input to the multiplexer output MO with $C_j=0$ for $j<i$ and $P_{3b}=P_{1b}$. Finally, consider the path $P_4=P_{4a}/P_{4b}$ of the 1st category, where P_4 belongs to the group of weight 0 and $P_{4a}=P_{3a}$ and $P_{4b}=P_{2b}$. From the above analysis we can see that the propagation delay $d(P_1)$ along path P_1 can be expressed as a linear combination of the propagation delays $d(P_2)$, $d(P_3)$ and $d(P_4)$ along paths P_2, P_3 and P_4 respectively, as : $d(P_1) = d(P_2) + d(P_3) - d(P_4)$. Note that the paths P_3 and P_4 are established for the same values of t_1t_0 as P_1. The fact that the path P_2 has been measured with $t_1t_0=00$ does not invalidate our results since the propagation delay along sub-paths P_{2b}, P_{4b} is independent of the values of t_1t_0. ▪

3rd Category. Paths starting from the function inputs.

In this case we have to measure the propagation delays along paths with input t_0 or t_1 and output one of the primary outputs of the shifter for constant values at the data inputs and $C_{m-1}C_{m-2} \ldots C_0$. Since t_0 and t_1 drive all levels of the shifter there are non-robustly testable paths. For example the path with input t_0 and output R_3 in Figure 1 for $t_1=0$, $C_0=C_1=1$, $C_2=0$ and $B_0=0$ and $B_2=1$ is non-robustly testable because the AND gate in the multiplexer with label 3 in level 1, that belongs on the path is driven also by t_0. The same is valid for the paths where more than one of the signals $C_{m-1}C_{m-2} \ldots C_0$ are equal to 1.

Let M_i and Q_i be the sets of all paths starting from t_0 and t_1 respectively with $C_i=1$ and all the other control signals $C_j=0$, with $j \neq i$. The measurement of the propagation delays along the paths of M_i and Q_i for $i=0, 1, 2, \ldots, \log_2 n-1$ can be done as the paths of L_i in case 2. Specifically holding the data inputs to the values : 2^i zeroes, 2^{i+1} ones, 2^{i+1} zeroes, 2^{i+1} ones … and 2^i ones, 2^{i+1} zeroes, 2^{i+1} ones, 2^{i+1} zeroes … for each transition 0->1 and 1->0 of t_0 and t_1, we measure the propagation delays of all paths belonging to M_i and Q_i.

The propagation delays along any other path not belonging to M_i or Q_i for $i = 0, 1, \ldots, \log_2 n - 1$ can be calculated as a function of the propagation delays of paths belonging to M_i or Q_i and two paths of the 1st category.

For example in Figure 1 the propagation delay along the path $P_1=t_0\text{-}O_4/O_4\text{-}P_2/P_2\text{-}R_2$ ($C_0=C_1=1$, $C_2=0$) can be calculated from the delays along the paths : $P_2=t_0\text{-}O_4/O_4\text{-}P_4/P_4\text{-}R_4$ ($C_0=1$, $C_1=C_2=0$, $t_1=0$, $t_0=T$, where T denotes a transition 0->1 or 1->0), $P_3=B_5\text{-}O_4/O_4\text{-}P_4/P_4\text{-}R_4$ ($C_0=1$, $C_1=C_2=0$, $t_1=t_0=0$), $P_4=B_5\text{-}O_4/O_4\text{-}P_2/P_2\text{-}R_2$ ($C_0=C_1=1$, $C_2=0$, $t_1=t_0=0$), as : $d(P_1) = d(P_2) + d(P_4) - d(P_3)$

For every level i the number of test sessions in order to measure the propagation delays along the paths in sets M_i and Q_i is 8. Thus in order to measure the propagation delay times along the paths in all sets M_i and Q_i, where $0 \leq i \leq m-1$, we need $8*\log_2 n$ test sessions.

From the above analysis we conclude that all possible paths of an n-bit shifter require $20*\log_2 n+2$ test sessions for path delay fault testing.

3. Conclusions

The number of all logical paths (physical paths * 2) of the shifter is $O(n^2)$, where n is the length of the shifter. Many of them are not robustly testable. In this paper we proposed a new path selection method so as all the selected paths to be robustly testable by $O(\log_2 n)$ test-vector pairs. We have also shown that the propagation along all the other paths can be calculated from the delays along the selected paths. Therefore the application of the proposed method reduces significantly the test application time.

References

[1] Z. Brazilai and B. Rosen, "Comparison of ac self - testing procedures", Proc. of ITC-83, pp. 560-571.

[2] K. D. Wagner, "The error latency of delay faults in combinational and sequential circuits", Proc. of ITC-85, pp. 334 - 341, Nov. 1985.

[3] G. L. Smith, "Model for delay faults based upon paths", Proc. of ITC - 85, pp. 342 - 349.

[4] W. K. Lam, et. al., "Delay fault coverage, test set size and performance trade-offs", IEEE Trans. On Computer Aided Design, vol. 14, no. 1, pp. 32 - 44, Jan. 1995.

[5] G. M. Luong and D. M. H. Walker, "Test generation for global delay faults", Proc. of ITC-96, pp. 433 - 442.

[6] S. Tani, et. al., "Efficient Path Selection for Delay Testing Based on Partial Path Evaluation", Proc. of 16th IEEE VLSI Test Symp., pp. 188 - 193, 1998.

[7] T. Haniotakis, Y. Tsiatouhas and D. Nikolos, "C-Testable One-Dimensional ILAs with Respect to Path Delay Faults : Theory and Applications", Proc. of 1998 IEEE Int. Symp. on Defect and Fault Tolerance in VLSI Systems, 2 - 4 November, 1998, Austin, Texas, pp. 155 –163.

[8] N. H. E. Weste and K. Eshraghian, Principles of CMOS VLSI Design, Addison - Wesley, 2nd edition, 1993.